



#3
11-7-97

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Application of:
Mailloux, et al.

Serial No.: 08/650,719

Filed: May 20, 1996

For: BURST/PIPELINED EDO MEMORY DEVICE

§
§ Group Art Unit: 2318
§
§ Examiner: Peikari, B. J.
§
§ Atty. Docket: 95-0653
§
§ Paper No. 2
§
§
§
§
§
§

INFORMATION DISCLOSURE STATEMENT

Assistant Commissioner for Patents
Washington, D.C. 20231

Dear Sir:

Certificate of Mailing (37 C.F.R. § 1.8)

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail, postage prepaid, in an envelope addressed to: Assistant Commissioner for Patents, Washington, D.C. 20231, on the date below:

10/31/97 Date
Geggy Lloyd Signature

In compliance with the duty of disclosure under 37 C.F.R. § 1.56, Applicant[s] respectfully request[s] that this Information Disclosure Statement be entered and that the references listed on the attached Form PTO-1449 be considered by the Examiner and made of record. Copies of the listed references are enclosed for the convenience of the Examiner.

In accordance with 37 C.F.R. § 1.97(b), this Information Disclosure Statement is not to be construed as a representation that a search has been made or that no other possible material information as defined in 37 C.F.R. § 1.56(a) exists.

The following references are submitted for the Examiner's review:

U.S. Patents

<u>U.S. Patent No.</u>	<u>Issue Date</u>	<u>Inventor</u>
5,357,469	10/18/94	Sommer et al.
5,268,865	12/7/93	Takasugi
4,618,947	10/21/86	Tran et al.
5,267,200	11/30/93	Tobita
4,344,156	8/10/82	Eaton et al.
4,707,811	11/17/87	Takemae et al.
4,649,522	3/10/87	Kirsch

4,603,403	7/29/86	Toda
4,567,579	1/28/86	Patel et al.
4,484,308	11/20/84	Lewandowski et al.
4,875,192	10/17/89	Matsumoto
4,685,089	8/4/87	Patel et al.
4,562,555	12/31/85	Ouchi et al.
4,575,825	3/11/86	Ozaki et al.
4,788,667	11/29/88	Nakano
5,392,239	2/21/95	Margulis et al.
5,379,261	1/3/95	Jones, Jr.
5,126,975	6/30/92	Handy et al.
5,331,593	7/94	Merritt
5,331,471	5/90	Matsumoto
5,526,320	6/11/96	Zagar et al.
5,268,865	12/93	Takasugi
5,319,759	6/94	Chan
5,327,390	7/94	Takasugi
5,426,606	6/95	Takai
5,369,622	11/94	McLaury

Other References

Samsung Electronics, "Samsung Synchronous DRAM", March 1993, pgs. 1-16

Oki Electric Ind. Co., Ltd., "Burst DRAM Function & Pinout", 2nd presentation, Item #619, September, 1994

Toshiba America Electronic Components, Inc., "Application Specific DRAM, 1994", Pgs. C-178, C-260, C218

Micron Semiconductor, Inc., "Synchronous DRAM 2 MEG x 8 SDRAM", Pgs. 2-43 through 2-83

Toshiba America Electronic Components, Inc., "4M DRAM 1991", Pgs. A-137 - A-159

Micron Semiconductor, Inc., "1994 DRAM Data Book", pgs. 2-1 to 2-6

Mosel-Vitellic V53C8257H DRAM Specification Sheet, 20 pgs.

Toshiba Corp., "Integrated Circuit Technical Data-262,144 Words x 8 Bits Multiport DRAM", TC52826TS/Z/FT/TR-1, TEN. Rev. 2.1

Micron Technology, Inc., "Burst EDO DRAM Information", pgs. 1-126, Rev. 9/95

Micron Semiconductor, Inc., "Synchronous DRAM 4 Meg x 4 SDRAM", Pgs. 2-1 to 2-2
Micron Technology, Inc., "1996 DRAM Data Book", Pgs. 1-1 to 1-52, and 4-1 to 4-42

Micron Technology, Inc., "1995 DRAM Data Book", Pgs. 3-1 to 3-37

"Hyper Page Mode DRAM", 8029 Electronic Engineering, 66, No. 813, Woolwich, London, GB, pp. 47-48, (September 1994)

Dave Bursky, "Novel I/O Options and Innovative Architectures Let DRAMs Achieve SRAM

Performance; Fast DRAMS can be swapped for SRAM Caches", Electronic Design, Vol. 41, No. 15, Cleveland, Ohio, pp. 55-67, (July 22, 1993)

Shiva P. Gowni, et al., "A 9NS, 32K X 9, BICMOS TTL Synchronous Cache RAM With Burst Mode

Access", IEEE, Cutsom Integrated Circuits Conference, pp. 781-786, (March 3, 1992) S3 Incorporated, "S3 Burst Mode DRAM", 6/93, 2 pages

Electronic News "Mitsubishi Samples 16M Synch DRAM", 10/25/93, pgs. 3-4

"DRAM 1 Meg X 4 DRAM 5BEDO Page Mode",", 1995 DRAM Data Book, pp.1-1 thru 1-30,, (Micron Technology, I)

NEC "Command Truth Table" March 15, 1993

Samsung Electronics "KM48SV2000 Preliminary CMOS SDRAM" Rev.1(Mar, 1993), pgs. 7-8

This Information disclosure Statement is being submitted after the mailing of the first Office Action, but before the mailing of a Final Rejection or Notice of Allowance. The Commissioner is authorized to charge the fee set forth in 37 C.F.R. § 1.17(p) of \$240.00 and any additional fees which may be required to Micron Technology, Inc. Deposit Account No. 13-3092, Order No. 97-0242.00.

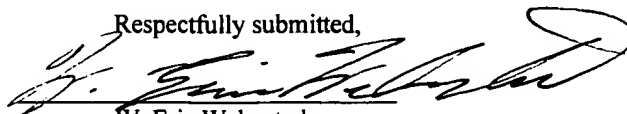
If there are any matters which may be resolved or clarified through telephone interview, the Examiner is respectfully requested to contact Applicant's undersigned attorney at the number indicated.

* * * *

A Form PTO-1449 is enclosed herewith.

Date: 10-30-97

Respectfully submitted,



W. Eric Webostad
Reg. No. 35,406
Micron Technology, Inc.
8000 S. Federal Way
Boise, ID 83706-9632
(208) 368-4792